



Reconfigurable and Adaptive Computing: Theory and Applications

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Reconfigurable computing techniques and adaptive systems are some of the most promising architectures for microprocessors. **Reconfigurable and Adaptive Computing: Theory and Applications** explores the latest research activities on hardware architecture for reconfigurable and adaptive computing systems.

The first section of the book covers reconfigurable systems. The book presents a software and hardware codesign flow for coarse-grained systems-on-chip, a video watermarking algorithm for the H.264 standard, a solution for regular expressions matching systems, and a novel field programmable gate array (FPGA)-based acceleration solution with MapReduce framework on multiple hardware accelerators.

The second section discusses network-on-chip, including an implementation of a multiprocessor system-on-chip platform with shared memory access, end-to-end quality-of-service metrics modeling based on a multi-application environment in network-on-chip, and a 3D ant colony routing (3D-ACR) for network-on-chip with three different 3D topologies.

The final section addresses the methodology of system codesign. The book introduces a new software–hardware codesign flow for embedded systems that models both processors and intellectual property cores as services. It also proposes an efficient algorithm for dependent task software–hardware codesign with the greedy partitioning and insert scheduling method (GPISM) by task graph.



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